## ABSTRACT OF THE DISCLOSURE

A flip-flop circuit includes a latch that holds an input signal responsive to an internal clock signal, a comparing circuit that compares the input signal with a latch output to provide a comparison signal, and an internal clock generator that receives an external clock signal and generates an internal clock signal responsive to the comparison signal. The internal clock generating circuit performs a NAND operation on the external clock signal and a delayed inverted version of the external clock signal, to generate the internal clock signal having pulse width smaller than the external clock signal and having rising and falling edges synchronized with the external clock signal. Power consumption is low because the clock buffer and the internal clock generating circuit do not perform switching operations when there is little or no variation in the input signal of the flip-flop.